74AUP2G79

Low-power dual D-type flip-flop; positive-edge trigger

Rev. 02 — 19 March 2008 Product data sheet

1. General description

The 74AUP2G79 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

The 74AUP2G79 provides the dual positive-edge triggered D-type flip-flop. Information on the data input (nD) is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse (nCP). The nD input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

2. Features

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E Class 3A exceeds 5000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101-C exceeds 1000 V
- Low static power consumption; I_{CC} = 0.9 µA (maximum)
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from –40 °C to +85 °C and –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G79DC	–40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AUP2G79GT	–40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74AUP2G79GM	–40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm	SOT902-1

4. Marking

Table 2. Marking codes

Type number	Marking code
74AUP2G79DC	p79
74AUP2G79GT	p79
74AUP2G79GM	p79

5. Functional diagram

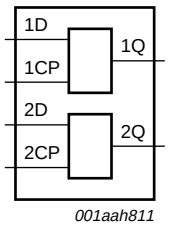


Fig 1. Logic symbol

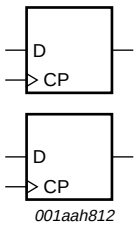


Fig 2. IEC logic symbol

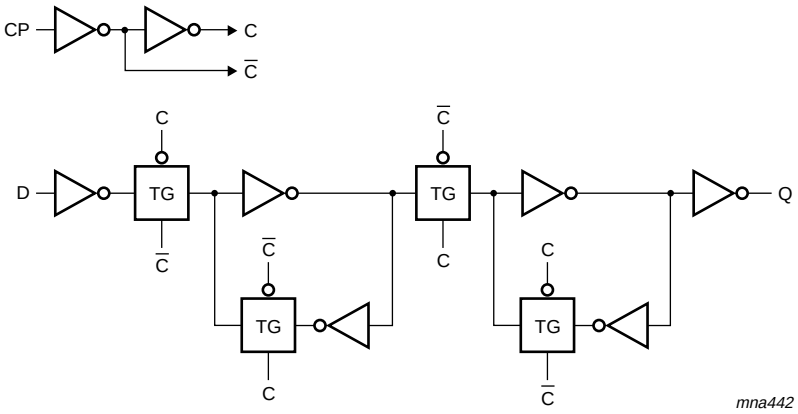


Fig 3. Logic diagram (one flip-flop)

6. Pinning information

6.1 Pinning

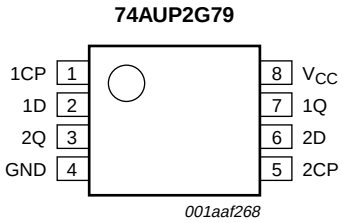


Fig 4. Pin configuration SOT765-1 (VSSOP8)

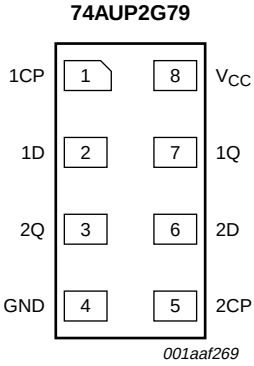


Fig 5. Pin configuration SOT833-1 (XSON8)

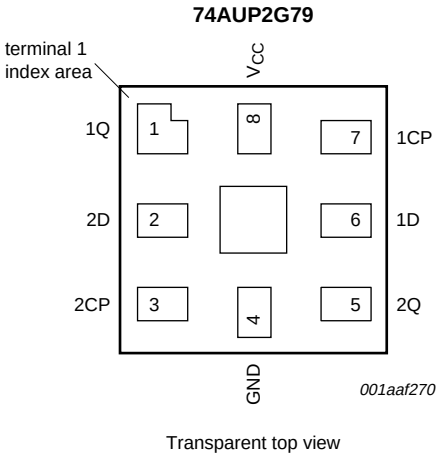


Fig 6. Pin configuration SOT902-1 (XQFN8U)

6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT765-1 and SOT833-1	SOT902-1	
1CP	1	7	clock pulse input 1
1D	2	6	data input 1
2Q	3	5	data output 2
GND	4	4	ground (0 V)
2CP	5	3	clock pulse input 2
2D	6	2	data input 2
1Q	7	1	data output 1
V_{CC}	8	8	supply voltage

7. Functional description

Table 4. Function table[1]

Input		Output
nCP	**nD**	**nQ**
↑	L	L
↑	H	H
L	X	q

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
X = don't care;
q = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-	–50	mA
V_I	input voltage		[1]	–0.5	+4.6	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode and Power-down mode	[1]	–0.5	+4.6	V
I_O	output current	V_O = 0 V to V_{CC}		-	±20	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-	–50	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8 and XQFN8U packages: above 45 °C the value of P_{tot} derates linearly with 2.4 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	3.6	V
T_{amb}	ambient temperature		–40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 0.8 V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = 25 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V		0.70 × V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V		0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V		-	-	0.30 × V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V		-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V		-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = –20 µA; V_{CC} = 0.8 V to 3.6 V		V_{CC} – 0.1	-	-	V
		I_O = –1.1 mA; V_{CC} = 1.1 V		0.75 × V_{CC}	-	-	V
		I_O = –1.7 mA; V_{CC} = 1.4 V		1.11	-	-	V
		I_O = –1.9 mA; V_{CC} = 1.65 V		1.32	-	-	V
		I_O = –2.3 mA; V_{CC} = 2.3 V		2.05	-	-	V
		I_O = –3.1 mA; V_{CC} = 2.3 V		1.9	-	-	V
		I_O = –2.7 mA; V_{CC} = 3.0 V		2.72	-	-	V
		I_O = –4.0 mA; V_{CC} = 3.0 V		2.6	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V		-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V		-	-	0.3 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V		-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V		-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V		-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V		-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V		-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V		-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V		-	-	±0.1	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V		-	-	±0.2	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V		-	-	±0.2	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V		-	-	0.5	µA
ΔI_{CC}	additional supply current	per pin; V_I = V_{CC} – 0.6 V; I_O = 0 A; V_{CC} = 3.3 V	[1]	-	-	40	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND or V_{CC}		-	0.6	-	pF
C_O	output capacitance	V_O = GND; V_{CC} = 0 V		-	1.3	-	pF

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	0.70 × V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V	0.65 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	0.30 × V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V	-	-	0.35 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} − 0.1	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	0.7 × V_{CC}	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.03	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.30	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	1.97	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.85	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.67	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	0.3 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.37	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.35	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.33	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.6	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.9	µA
ΔI_{CC}	additional supply current	per pin; V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	50	µA

Table 7. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C							
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V		0.75 × V_{CC}	-	-	V
		V_{CC} = 0.9 V to 1.95 V		0.70 × V_{CC}	-	-	V
		V_{CC} = 2.3 V to 2.7 V		1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V		-	-	0.25 × V_{CC}	V
		V_{CC} = 0.9 V to 1.95 V		-	-	0.30 × V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V		-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V		-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = −20 µA; V_{CC} = 0.8 V to 3.6 V		V_{CC} − 0.11	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V		0.6 × V_{CC}	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V		0.93	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V		1.17	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V		1.77	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V		1.67	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V		2.40	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V		2.30	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}					
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V		-	-	0.11	V
		I_O = 1.1 mA; V_{CC} = 1.1 V		-	-	0.33 × V_{CC}	V
		I_O = 1.7 mA; V_{CC} = 1.4 V		-	-	0.41	V
		I_O = 1.9 mA; V_{CC} = 1.65 V		-	-	0.39	V
		I_O = 2.3 mA; V_{CC} = 2.3 V		-	-	0.36	V
		I_O = 3.1 mA; V_{CC} = 2.3 V		-	-	0.50	V
		I_O = 2.7 mA; V_{CC} = 3.0 V		-	-	0.36	V
		I_O = 4.0 mA; V_{CC} = 3.0 V		-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V		-	-	±0.75	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V		-	-	±0.75	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V		-	-	±0.75	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V		-	-	1.4	µA
ΔI_{CC}	additional supply current	per pin; V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 3.3 V	[1]	-	-	75	µA

[1] One input at V_{CC} − 0.6 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 5 pF										
t_{pd}	propagation delay	nCP to nQ; see Figure 7 [2]								
		V_{CC} = 0.8 V	-	19.7	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	2.6	5.5	11.0	2.4	12.9	2.4	14.2	ns
		V_{CC} = 1.4 V to 1.6 V	2.0	3.8	7.0	1.8	8.1	1.8	9.0	ns
		V_{CC} = 1.65 V to 1.95 V	1.7	3.1	5.4	1.5	6.4	1.5	7.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	2.3	4.0	1.1	4.7	1.1	5.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	2.0	3.4	0.9	4.0	0.9	4.4	ns
f_{max}	maximum frequency	nCP; see Figure 8								
		V_{CC} = 0.8 V	-	53	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V	-	203	-	170	-	170	-	MHz
		V_{CC} = 1.4 V to 1.6 V	-	347	-	310	-	300	-	MHz
		V_{CC} = 1.65 V to 1.95 V	-	435	-	400	-	390	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	550	-	490	-	480	-	MHz
		V_{CC} = 3.0 V to 3.6 V	-	619	-	550	-	510	-	MHz
C_L = 10 pF										
t_{pd}	propagation delay	nCP to nQ; see Figure 7 [2]								
		V_{CC} = 0.8 V	-	23.1	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.1	6.3	12.3	2.8	14.4	2.8	15.9	ns
		V_{CC} = 1.4 V to 1.6 V	2.5	4.4	8.1	2.2	9.5	2.2	10.5	ns
		V_{CC} = 1.65 V to 1.95 V	2.1	3.6	6.3	1.9	7.5	1.9	8.3	ns
		V_{CC} = 2.3 V to 2.7 V	1.8	2.8	4.7	1.5	5.6	1.5	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.7	2.5	4.1	1.3	4.5	1.3	5.0	ns
f_{max}	maximum frequency	nCP; see Figure 8								
		V_{CC} = 0.8 V	-	52	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V	-	192	-	150	-	150	-	MHz
		V_{CC} = 1.4 V to 1.6 V	-	324	-	280	-	230	-	MHz
		V_{CC} = 1.65 V to 1.95 V	-	421	-	310	-	250	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	486	-	370	-	360	-	MHz
		V_{CC} = 3.0 V to 3.6 V	-	550	-	410	-	360	-	MHz

Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 15 pF										
t_{pd}	propagation delay	nCP to nQ; see Figure 7 [2]								
		V_{CC} = 0.8 V	-	26.6	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.5	7.1	13.6	3.2	15.6	3.2	17.2	ns
		V_{CC} = 1.4 V to 1.6 V	2.8	5.0	9.2	2.5	10.7	2.5	11.8	ns
		V_{CC} = 1.65 V to 1.95 V	2.4	4.1	7.1	2.2	8.5	2.2	9.4	ns
		V_{CC} = 2.3 V to 2.7 V	2.2	3.2	5.4	1.9	6.3	1.9	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	2.0	2.9	4.5	1.6	5.0	1.6	5.5	ns
f_{max}	maximum frequency	nCP; see Figure 8								
		V_{CC} = 0.8 V	-	50	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V	-	181	-	120	-	120	-	MHz
		V_{CC} = 1.4 V to 1.6 V	-	301	-	190	-	160	-	MHz
		V_{CC} = 1.65 V to 1.95 V	-	407	-	240	-	190	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	422	-	300	-	270	-	MHz
		V_{CC} = 3.0 V to 3.6 V	-	481	-	320	-	300	-	MHz
C_L = 30 pF										
t_{pd}	propagation delay	nCP to nQ; see Figure 7 [2]								
		V_{CC} = 0.8 V	-	36.8	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	4.7	9.3	17.3	4.2	23.3	4.2	25.6	ns
		V_{CC} = 1.4 V to 1.6 V	3.8	6.4	11.8	3.3	14.3	3.3	15.7	ns
		V_{CC} = 1.65 V to 1.95 V	3.3	5.3	9.4	3.0	11.3	3.0	12.4	ns
		V_{CC} = 2.3 V to 2.7 V	3.0	4.3	7.0	2.7	8.5	2.7	9.4	ns
		V_{CC} = 3.0 V to 3.6 V	2.8	3.9	5.8	2.6	7.2	2.6	7.9	ns
f_{max}	maximum frequency	nCP; see Figure 8								
		V_{CC} = 0.8 V	-	28	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V	-	128	-	70	-	70	-	MHz
		V_{CC} = 1.4 V to 1.6 V	-	206	-	120	-	110	-	MHz
		V_{CC} = 1.65 V to 1.95 V	-	262	-	150	-	120	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	269	-	190	-	170	-	MHz
		V_{CC} = 3.0 V to 3.6 V	-	309	-	200	-	190	-	MHz

Table 8. Dynamic characteristics *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
t_{su}	set-up time	HIGH; nD to nCP; see Figure 8								
		V_{CC} = 0.8 V	-	3.4	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	0.8	-	1.5	-	1.5	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	0.5	-	1.0	-	1.0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	0.5	-	0.9	-	0.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.4	-	0.7	-	0.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.4	-	0.6	-	0.6	-	ns
		LOW; nD to nCP; see Figure 8								
		V_{CC} = 0.8 V	-	3.0	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	0.9	-	1.6	-	1.6	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	0.6	-	1.0	-	1.0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	0.5	-	0.9	-	0.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.5	-	0.9	-	0.9	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.7	-	1.0	-	1.0	-	ns
t_h	hold time	nD to nCP; see Figure 8								
		V_{CC} = 0.8 V	-	–1.9	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	–0.6	-	0	-	0	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	–0.4	-	0	-	0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	–0.4	-	0	-	0	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	–0.4	-	0	-	0	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	–0.3	-	0	-	0	-	ns
t_W	pulse width	HIGH or LOW; nCP; see Figure 8								
		V_{CC} = 0.8 V	-	5.6	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	2.4	-	3.5	-	3.5	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	1.3	-	2.0	-	2.0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	0.9	-	1.9	-	1.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.7	-	2.0	-	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.6	-	2.2	-	2.2	-	ns

Table 8. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 9.

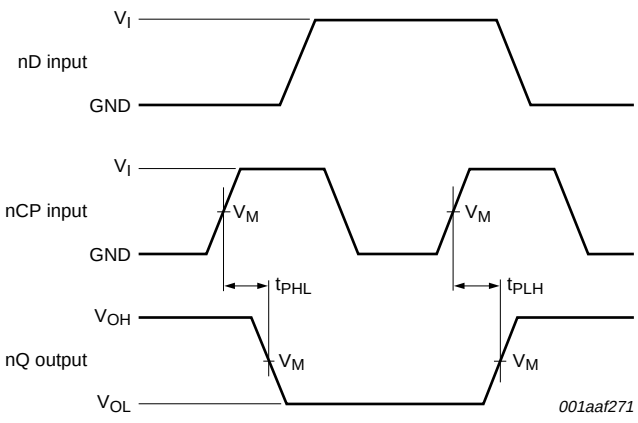
Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	f = 1 MHz; V_I = GND to V_{CC} [3]								
		V_{CC} = 0.8 V	-	1.6	-	-	-	-	-	pF
		V_{CC} = 1.1 V to 1.3 V	-	1.7	-	-	-	-	-	pF
		V_{CC} = 1.4 V to 1.6 V	-	1.8	-	-	-	-	-	pF
		V_{CC} = 1.65 V to 1.95 V	-	1.9	-	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	2.3	-	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	2.7	-	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

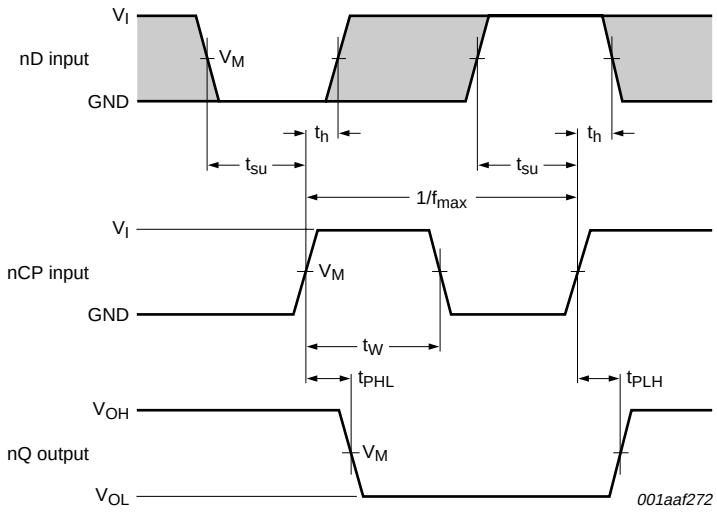
12. Waveforms



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. The clock input (nCP) to output (nQ) propagation delays



Measurement points are given in Table 9.

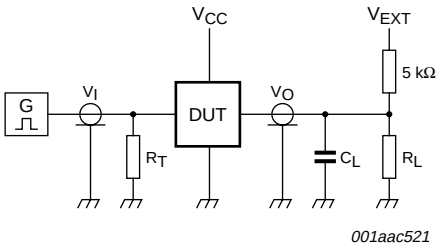
Logic levels: V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 8. The clock input (nCP) to output (nQ) propagation delays, nCP clock pulse width, nD to nCP set-up times, nCP to nD hold times and the nCP maximum frequency

Table 9. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns



Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 9. Load circuitry for switching times

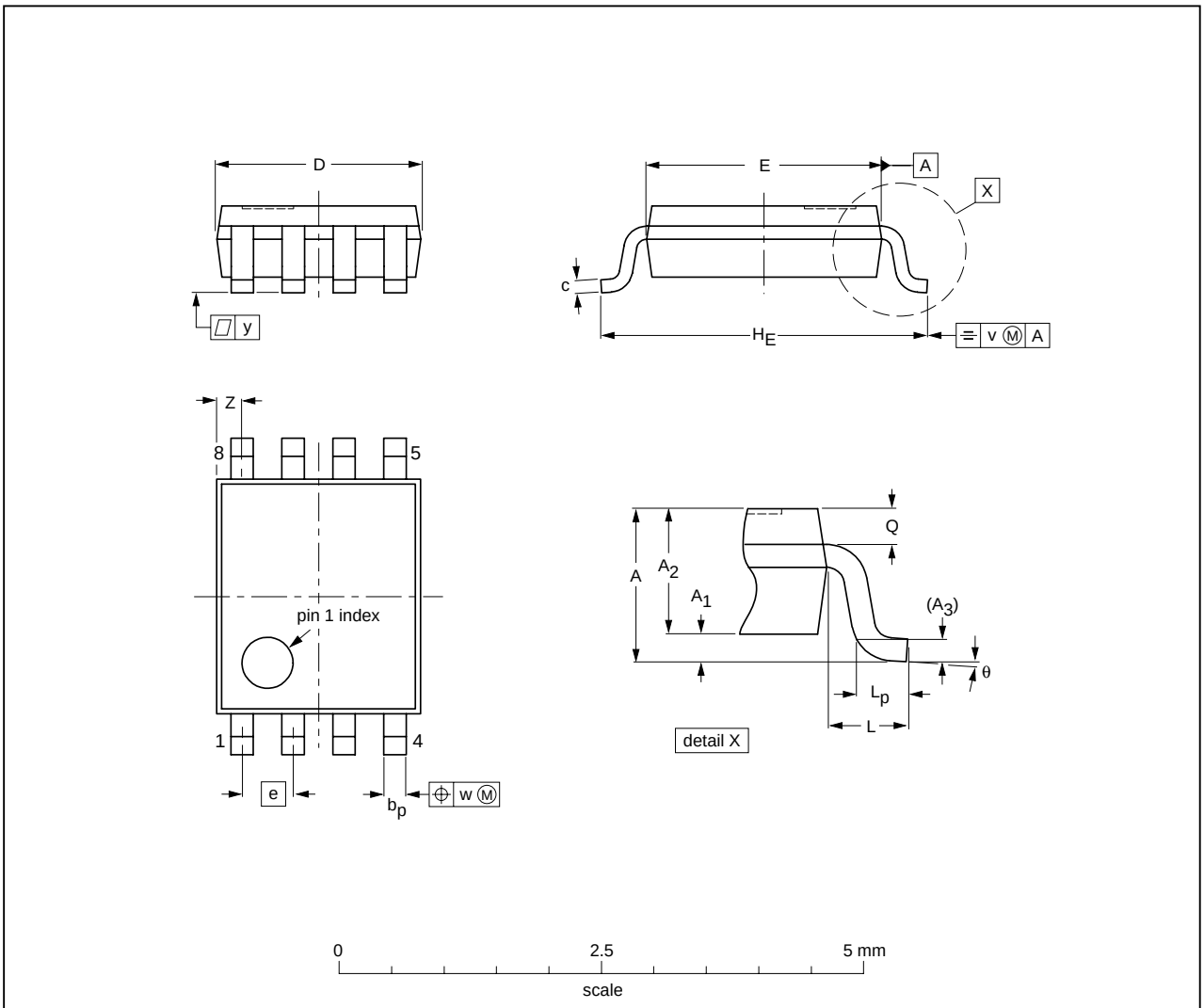
Table 10. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times R_L = 5 kΩ.
For measuring propagation delays, set-up times, hold times and pulse width, R_L = 1 MΩ.

13. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm **SOT765-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

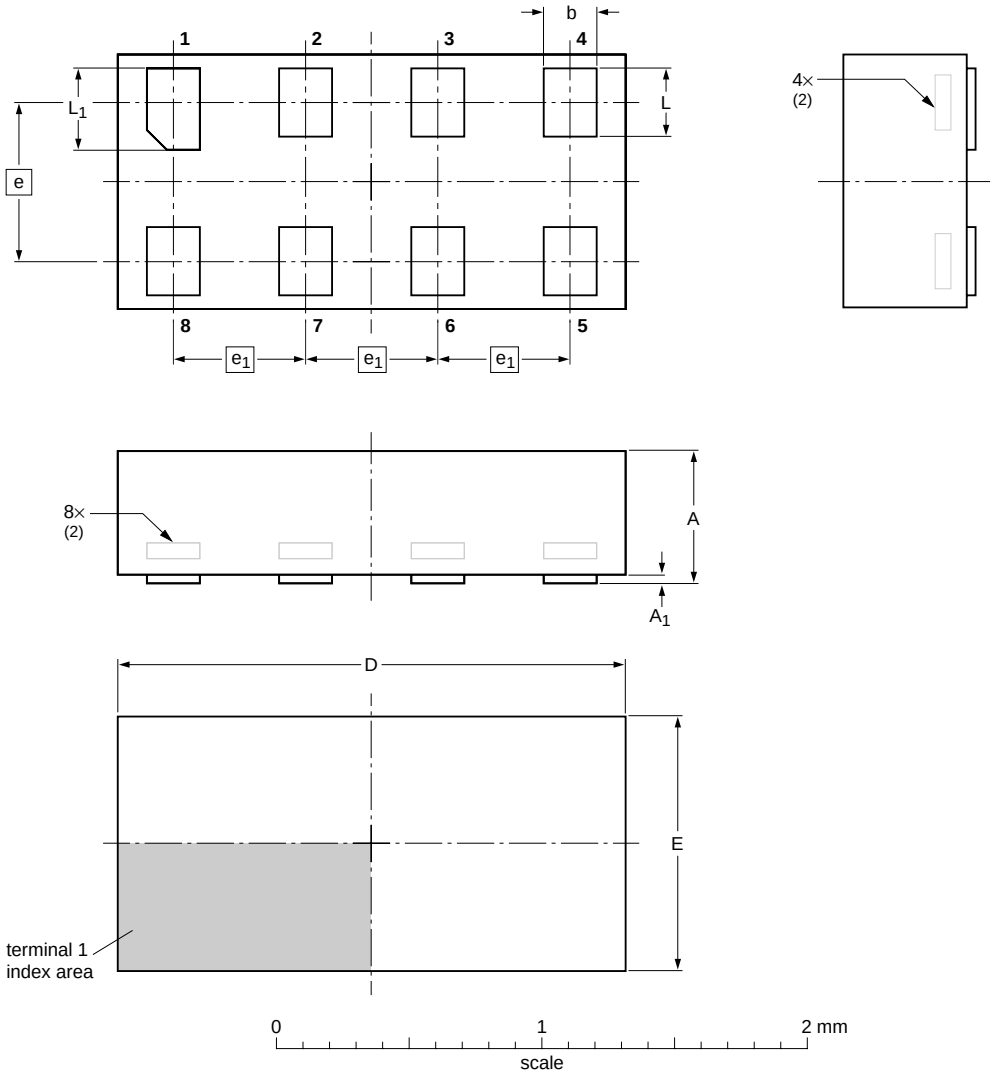
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

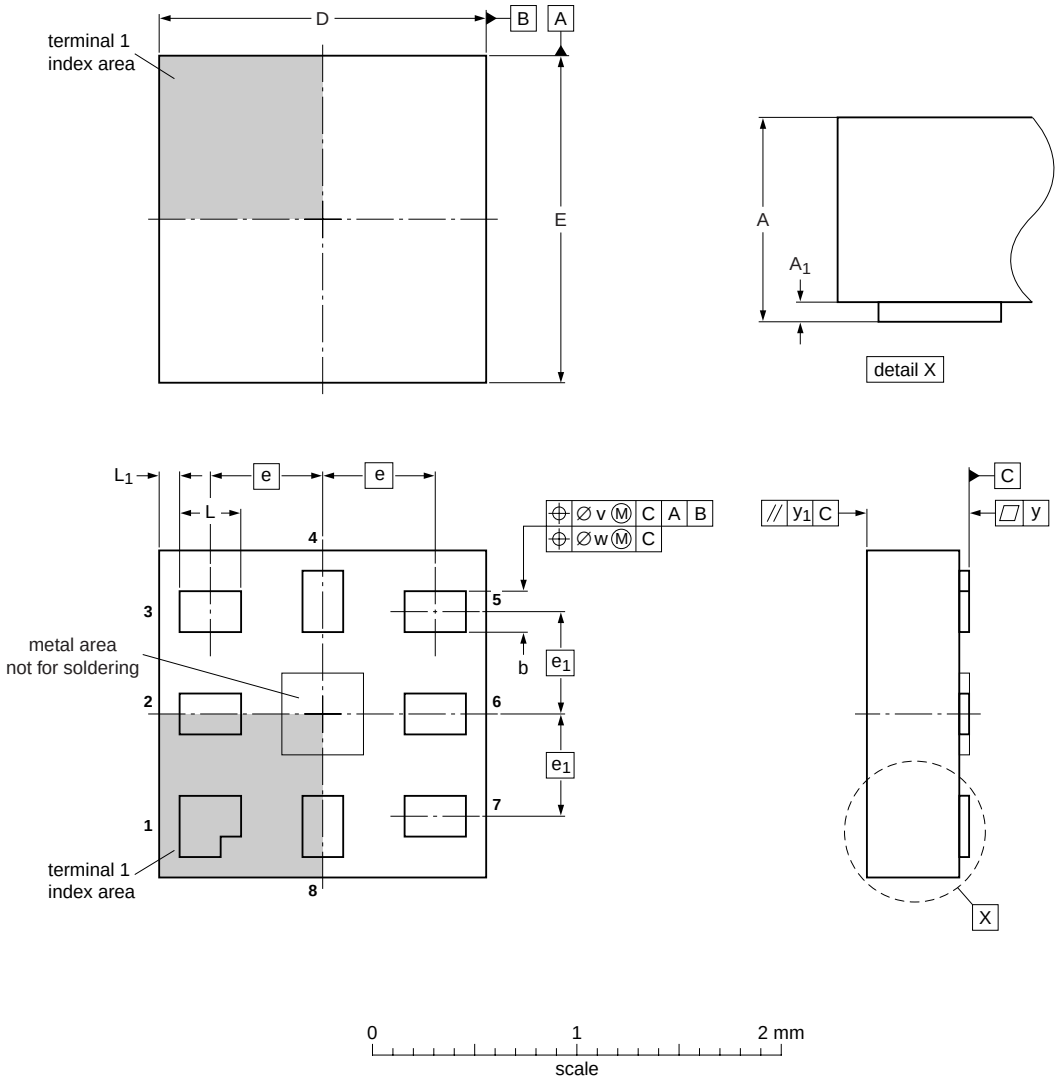
Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 11. Package outline SOT833-1 (XSON8)

XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm **SOT902-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	0.5	0.05 0.00	0.25 0.15	1.65 1.55	1.65 1.55	0.55	0.5	0.35 0.25	0.15 0.05	0.1	0.05	0.05	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT902-1	- - -	MO-255	- - -			~~05-11-25~~ 07-11-14

Fig 12. Package outline SOT902-1 (XQFN8U)

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G79_2	20080319	Product data sheet	-	74AUP2G79_1
Modifications:	• Figure 1 and Figure 2: pin numbers removed from logic symbols • Figure 12: package outline drawing updated to latest version			
74AUP2G79_1	20061006	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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